WHAT IS CLAIMED IS:

1. A method of fabricating a MOSFET device, comprising:

forming a gate structure on a substrate, said gate structure comprising a gate dielectric layer and a conductive layer;

forming a masking layer to cover said gate structure and the substrate;

etching said masking layer to expose a side of said gate structure and a region of a surface of the substrate adjacent to the side;

performing an oxidation process on part of the exposed side of said gate structure, such that a bottom corner of the exposed gate structure is oxidized to form a bird's beak structure;

removing said masking layer; and

forming a source region and a drain region in the substrate respectively adjacent to two sides of said gate structure, wherein said drain region is adjacent to said bird's beak structure and the exposed side.

2. The method of claim 1, wherein said conductive layer comprises a polysilicon layer.

3. The method of claim 2, further comprising laterally etching part of said gate dielectric layer on the exposed side before performing said oxidation process.

4. The method of claim 3, wherein the lateral etching step is performed

by isotropic etching.

5. The method of claim 1, wherein said gate dielectric layer comprises an oxide layer.

6. The method of claim 1, wherein said masking layer comprises a nitride layer.

7. The method of claim 1, wherein said masking layer comprises a silicon nitride layer.

8. A method of fabricating a MOSFET device, comprising:

forming a gate structure on a substrate, said gate structure comprising a gate dielectric layer and a conductive layer;

forming a masking layer to cover said gate structure and the substrate;

directing implant ions onto said masking layer at an angle so as to shield part of said masking layer against the ions;

selectively etching said masking layer so as to expose a side of said gate structure and a region of a surface of the substrate adjacent to the side;

performing an oxidation process on part of the exposed side of said gate structure, such that a bottom corner of the exposed gate structure is oxidized to form a bird's beak structure;

removing said masking layer; and

forming a source region and a drain region in the substrate respectively adjacent to two sides of said gate structure, wherein said drain region is adjacent to said bird's beak structure and the exposed side.

9. The method of claim 8, wherein said conductive layer comprises a polysilicon layer.

10. The method of claim 8, wherein said gate dielectric layer comprises an oxide layer.

11. The method of claim 8, wherein said masking layer comprises an oxide layer.

12. The method of claim 11, wherein forming said masking layer is performed by chemical vapor deposition.

13. The method of claim 8, wherein the selective etching comprises a wet etching process.

14. The method of claim 8, wherein said masking layer comprises a silicon dioxide layer.

15. The method of claim 14, wherein the selective etching comprises utilizing a solution comprising HF.

16. The method of claim 8, wherein the projected ions comprise one of nitrogen ions and argon ions.

17. The method of claim 8, further comprising laterally etching part of said gate dielectric layer on the exposed side before performing said oxidation process.

18. The method of claim 17, wherein the lateral etching step is performed by isotropic etching.

19. A MOSFET structure, comprising:

a substrate;

a gate dielectric layer on said substrate;

a gate on said gate dielectric layer;

a source region in said substrate, said source region being adjacent to said gate; and

a drain region in said substrate, said drain region being adjacent to said gate,

wherein a portion of said gate dielectric layer adjacent to said drain region has a bird's beak structure, so as to reduce the gate-to-drain overlap capacitance between said gate and said drain region.

20. The structure of claim 19, wherein said gate comprises a polysilicon layer.

21. The structure of claim 19, wherein said gate dielectric layer comprises an oxide layer.